	Туре	L#	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	5172	(716/).CCLS.	USPA T; US-P GPUB	2003/07/2 8 14:00
2	IS&R	L2	633	(716/6).CCLS.	USPA T; US-P GPUB	2003/07/2 8 14:02
3	BRS	L3	22	<pre>(layout same schematic) and (verification same design) and (resistance or capacitance) same extract</pre>	USPA T; US-P GPUB	2003/07/2 8 14:03
4	BRS	L4	3054	embedded same (structure or device) same logic	USPA T; US-P GPUB	2003/07/2 8 14:04
5	BRS	L5	646	delay same (clock-to-output or interconnect) same clock	USPA T; US-P GPUB	2003/07/2 8 14:02
6	BRS	L6	29047	path same timing	USPA T; US-P GPUB	2003/07/2 8 14:03
7	BRS	L7	0	2 and 3 and 4 and 5		2003/07/2 8 14:03
8	BRS	L8	0	3 and 4 and 5 and 6		2003/07/2 8 14:03
9	BRS	L9	O	3 and 4 and 5		2003/07/2 8 14:03
10	BRS	L10	0	3 and 4		2003/07/2 8 14:03
11	BRS	L11	2	3 and 5		2003/07/2 8 14:03
12	BRS	L12	176	5 and 6		2003/07/2 8 14:04

	Туре	L#	Hits	Search Text	DBs	Time Stamp	
13	BRS	L14	253	4 and 6	:	2003/07/2 8 14:04	
14	BRS	L13	17	4 and 5		2003/07/2 8 14:09	
15	IS&R	L15	6	,		2003/07/2 8 14:11	